CLAIMS

What is claimed is:

1. A semiconductor device, comprising:

an active region in a semiconductor substrate;

a gate finger over a channel in the active region and spaced from the channel by a gate dielectric having a first thickness, wherein the gate finger is of a first material;

a first gate tab adjacent to the gate finger, over the active region and spaced from the substrate by a first tab insulator having a second thickness, wherein the first gate tab is of the first material and the second thickness is greater than the first thickness, wherein the first material is conductive;

a second gate tab adjacent to the gate finger, over the active region and spaced from the substrate by a second tab insulator having the second thickness, wherein the second gate tab is of the first material;

a first tab connection electrically connecting the first gate tab to the gate finger, wherein the first tab connection is of the first material;

a second tab connection electrically connecting the second gate tab to the gate finger, wherein the second gate tab is of the first material; and

a gate bus electrically connected to the first and second gate tabs.

2. The semiconductor device of claim 1, wherein the first material comprises polysilicon and the gate bus comprises a first metal.

3. The semiconductor device of claim 1, further comprising:

a first gate bus extension comprising the first metal, having a portion over the first gate tab, and making electrical contact to the first gate tab and the gate bus; and

a second gate bus extension comprising the first metal, having a portion over the second gate tab, and making electrical contact to the second gate tab and the gate bus.

4. The semiconductor device of claim 3, further comprising:

a lightly-doped drain region adjacent to the gate bus; and

a heavily-doped drain contact region adjacent to the lightly-doped drain region.

5. The semiconductor device of claim 4, further comprising:

a second gate finger over a second channel in the active area and spaced from the second channel by a second gate dielectric having the first thickness, wherein the second gate finger is of the first material;

a second lightly-doped drain region adjacent to a first side of the second gate finger and adjacent to the heavily-doped drain contact region;

a third gate tab adjacent to the second gate finger and spaced from the substrate by a third tab insulator having the second thickness, wherein the third gate tab is of the first material;

a fourth gate tab adjacent to the second gate finger and spaced from the substrate by a fourth tab insulator having the second thickness, wherein the fourth gate tab is of the first material;

a third tab connection electrically connecting the third gate tab to the second gate finger, wherein the third tab connection is of the first material;

a fourth tab connection electrically connecting the fourth gate tab to the second gate finger, wherein the fourth tab connection is of the first material; and

a second gate bus electrically connected to the third and fourth gate tabs.

6. The semiconductor device of claim 5, further comprising:

a third gate bus extension comprising the first metal, having a portion over the third gate tab, and making electrical contact to the third gate tab and the second gate bus; and

a fourth gate bus extension comprising the first metal, having a portion over the fourth gate tab, and making electrical contact to the fourth gate tab and the second gate bus.

7. The semiconductor device of claim 6, wherein the first material comprises polysilicon and the second gate bus comprises a first metal.

8. The semiconductor device of claim 1, wherein the gate dielectric and the first and second tab insulators comprise oxide.

9. The semiconductor device of claim 1, wherein the first and second tab insulators comprise a low K dielectric.

10. The semiconductor device of claim 1, wherein the second thickness is at least about four times greater than the first thickness.

11. A method of forming a semiconductor device, comprising:

providing a semiconductor substrate having an active area;

forming an insulating layer over the active area;

selectively removing portions of the insulating layer to leave a plurality of tab insulators in the active area;

forming a gate dielectric over the active area;

forming a first layer over the gate dielectric;

patterning the first layer to form a gate finger, a plurality of gate tabs adjacent to the gate finger, and a plurality of tab connections connecting the plurality of gate tabs to the gate finger; and

connecting the plurality of gate tabs together.

12. The method of claim 11, wherein the connecting is further characterized as forming a metal line that is connected to the plurality of gate tabs.

13. The method of claim 12, wherein the tab insulators have a thickness greater than that of the gate dielectric.

14. The method of claim 13, wherein the thickness of the tab insulators is at least about four times greater than the thickness of the gate dielectric.

15. A semiconductor device, comprising:

a semiconductor substrate;

a gate finger spaced from the substrate by a gate dielectric having a first thickness;

a first gate tab adjacent to the gate finger and spaced from the substrate by a first tab insulator having a second thickness;

a second gate tab adjacent to the gate finger and spaced from the substrate by a second tab insulator having the second thickness;

a first tab connection connected to the first gate tab and the gate finger;

a second tab connection connected to the second gate tab; and

a gate bus connected to the first and second gate tabs.

16. The semiconductor device of claim 15 wherein the gate finger is over a channel and the first and second gate tabs are spaced from the channel.

17. The semiconductor device of claim 15, wherein the gate bus is connected to the first and second gate tabs through first and second gate bus extensions from the gate bus.

18. The semiconductor device of claim 15, wherein the gate bus is parallel to the gate finger.

19. The semiconductor device of claim 15, wherein the gate bus comprises a metal.

20. The semiconductor device of claim 15, wherein the gate finger comprises polysilicon.

21. The semiconductor device of claim 15, wherein the first and second tab insulators are at least about four times thicker than the gate dielectric.

22. The semiconductor device of claim 15, wherein the first and second tab insulators comprise oxide.

23. The semiconductor device of claim 15, wherein the first and second tab insulators comprise a low K dielectric.

24. In a semiconductor device having contacts to gate tabs over an active region and gate fingers spaced from the active region by a gate dielectric of a first thickness and connected to the gate tabs, the improvement comprising:

tab insulators between the tab connections and the substrate having a thickness greater than the gate dielectric.

25. The semiconductor device of claim 24, wherein the tab insulators have a thickness of at least about four times greater than the thickness of the gate dielectric.

26. The semiconductor device of claim 24, wherein the tab insulators comprise oxide.

27. The semiconductor device of claim 24, wherein the tab insulators comprise a low K dielectric.